APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,883	12/10/1999	THOMAS R. PUZAK	YO999-589	9397

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EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>10 December 1999 and 03 August 2000</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-22</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-22</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>10 December 1999</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)   4) ☐ Interview Summary (PTO-413) Paper No(s). _____.

2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u>.   6) ☐ Other: .

DETAILED ACTION

Patent Office Communiqué

This detailed action is directed to the acknowledgement of the patent office

receiving and beginning an examination of patent application, "Prefetching Using Future

Branch Path Information Derived From Branch Prediction" (patent office application

number: 09/458,883), being filed on December 10, 1999 and being assigned to Patent

Examiner William Wood.

Acknowledgement is made of patent office receiving paper, "Information

Disclosure Statement", being filed on August 3, 2000.

Information Disclosure Statement

1.   The information disclosure statement filed August 3, 2000 fails to comply with 37

CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each

publication or that portion which caused it to be listed; and all other information or that

portion which caused it to be listed. Item AC titled Simpkins does not appear to be in

any way related to the subject matter under consideration as the document is titled

"Uses of Estrogen Compounds For the Treatment of Disease". The information referred

to therein has not been considered. Also item AQ has been listed twice and therefore,

the second occurrence has not been considered.

Oath/Declaration

2.   The oath or declaration is defective. A new oath or declaration in compliance

with 37 CFR 1.67(a) identifying this application by application number and filing date is

required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
It does not identify the mailing or post office address of each inventor. A mailing or post office address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing or post office address should include the ZIP Code designation. The mailing or post office address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration for applicants Peter H. Oden, Daniel A. Prener and Mark Charney. A statement over applicant's signature providing a complete post office address is required.

Drawings

3.   The drawings are objected to because of informalities found on draft person's review. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4.   The disclosure is objected to because of the following informalities: lacks a Summary of the Invention section and lacks Cross-Reference to Related Applications section. Copending application 09/459,739 should be mentioned. Appropriate correction is required. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC
        (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)),
        "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are
        permitted to be submitted on compact discs.) or
        REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche
        Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
        (1) Field of the Invention.
        (2) Description of Related Art including information disclosed under 37 CFR 1.97 and
        1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is
        required on paper if the application discloses a nucleotide or amino acid sequence as
        defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an
        electronic document on compact disc).

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a_ patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5.   Claims 1, 6 and 12 are provisionally rejected under 35 U.S.C. 101 as claiming

the same invention as that of claims 1, 14 and 18 of copending Application No.

09/459,739. This is a provisional double patenting rejection since the conflicting claims

have not in fact been patented.

In regard to claim 1, claim 1 of the copending application requires a "prefetch trigger" instruction. If the broadest reasonable interpretation is taken, the claims of the instant application read upon the claims of the copending application. This prefetch trigger can be found in the instant application's "at least one prefetch instruction" on line 3 of claim 1. The prefetch instruction is the trigger to prefetch. The copending application fails to define the trigger operation in the independent claim 1. Furthermore, the copending application requires "an instruction that uses information prefetched" on line 6 of claim 1. This is found in line 6 of claim 1 of the instant application. The other limitations of the claims can be easily seen to be parallel for the two applications.

In regard to claim 6 of the instant application, the phrase "one or more branch instructions" of the instant claim is broadly interpreted as "a branch instruction" (one) as found in the copending application.

In regard to claim 12, claim 12 in the instant application and 18 in the copending application are the same except only directed toward an apparatus and are thus rejected as well.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6.   Claims 10, 11, 21 and 22 are provisionally rejected under the judicially created

doctrine of obviousness-type double patenting as being unpatentable over claims 16,

17, 33 and 34 of copending Application No. 09/459,739. Although the conflicting claims

are not identical, they are not patentably distinct from each other because of the

following reasons. This is a provisional obviousness-type double patenting rejection

because the conflicting claims have not in fact been patented.

In regard to claim 10 of the instant application, though not word for word identical

the claim clearly reads upon claim 16 of the copending application. Though the

limitation "high speed buffer" is not expressly stated in the copending application's

claim, it is revealed in claim 1 of the copending application where a high speed buffer is

mentioned. The field limitation is not mentioned in the copending application, however it

would have been obvious to one of ordinary skill in the art to implement a field to point

to the information to be prefetched since this is the most direct and well known method

for indicating information to be prefetched.

In regard to claim 11 of the instant application, though the limitation "high speed

buffer" is not expressly stated in the copending application's claim 17, it is revealed in

claim 1 of the copending application where a high speed buffer is mentioned. The field

limitation is not mentioned in the copending application, however it would have been

obvious to one of ordinary skill in the art to implement a field to point to the information

to be prefetched since this is the most direct and well known method for indicating

information to be prefetched.

In regard to claim 22 of the instant application, the rejection is the same as claim

11 above only the instant claim is directed toward claim 34 of the copending application.

In regard to claim 21 of the instant application, the rejection is the same as claim

10 above only the instant claim is directed toward claim 33 of the copending application.

Claim Rejections – 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7.   Claims 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. The claims are apparatus claims and yet dependent

upon method claims, and as such are hybrid claims. This lacks clarity. Appropriate

correction is required. Examiner believes this to be mistake on applicant's part and will

make a prior art rejection based under the assumption that the claims were supposed to

be dependent on claim 12.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (f) he did not himself invent the subject matter sought to be patented.

8.   Claims 1, 6 and 12 are rejected under 35 U.S.C. 102(f) because the applicant did

not invent the claimed subject matter. The inventive subject matter has been shown to

be the same as copending application 09/459,739 as discussed above. Clearly the

inventive entities of both inventions are not identical, and therefore one or more of the

inventors of either the instant application or the copending application did not invent the

claimed subject matter.

9.   Claims 1-5, 10, 12-16 and 21 are rejected under 35 U.S.C. 102(b) as being

anticipated by Yeh et al. (USPN 5,742,804).

In regard to claim 1, Yeh taught the following limitations:

[i)] *a system including a high speed buffer logically placed between memory and at*

least one processor unit, a method of executing an instruction stream stored in

the memory, wherein the instruction stream comprises a sequence of instructions

including at least one prefetch instruction that prefetches information from the

memory into the high speed buffer (column 2, lines 27-34)

[ii)] *generating first path data, wherein the first path data represents a first path*

from the prefetch instruction to an instruction that uses information prefetched by

the prefetch instruction (column 4, lines 8-23)

[iii)] *generating second path data, wherein the second path data represents a*

predicted second path of execution (column 6, lines 28-36; the execution path

mentioned here is the second generated path data)

^{iv)} *conditionally executing the prefetch instruction based upon a comparison operation that compares the first path data to the second path data to determine if the first path data falls within the predetermined second path* (column 6, lines 33-36; canceling the prefetched request is the same as conditionally executing a prefetch instruction)

In regard to claim 2, Yeh taught the additional limitation *wherein the first path data is derived from a compiler performing static compilation* (column 4, lines 49-53; column 6, lines 21-27).

In regard to claim 3, Yeh taught the limitation *wherein the second path data is derived from information characterizing dynamic execution of the sequence of instructions by the processor unit* (column 6, lines 28-33; second path is the execution path).

In regard to claim 4, Yeh taught the limitation *wherein prefetch instruction is added to the instruction stream for execution by the at least one processor unit upon determining that the first path falls within the predicted second path* (column 6, lines 28-37; the unneeded prefetch requests are cancelled and in this manner only the prefetch instruction which is needed is added to the instruction stream for actual execution).

In regard to claim 5, Yeh taught the additional limitation *upon determining that the first path does not fall within the predicted second path, omitting the prefetch instruction from the instruction stream executed by the processor unit* (column 6, lines 28-37).

In regard to claims 10 and 21, Yeh taught the additional limitation *wherein the prefetch instruction includes a field that identifies an instruction to prefetch from memory into the high speed buffer* (Figure 1, predict branch 6 instruction shown to have a "target" field; column 4, line 6).

In regard to claim 12, Yeh taught the following limitations

[i] *a system including a memory storing an instruction stream comprising a sequence of instructions including at least one prefetch instruction, a processor unit for executing the sequence of instructions, and a high speed buffer logically placed between the memory and the one processor unit, an apparatus for conditionally executing the prefetch instruction* (column 2, lines 27-34)

[ii] *decode logic for generating first path data, wherein the first path data represents a first path from the prefetch instruction to an instruction that uses information prefetched by the prefetch instruction* (column 4, lines 8-23; column 6, lines 21-27)

iii) *path prediction logic for generating second path data, wherein the second path*

data represents a predicted second path of execution (column 6, lines 28-36; the

execution path mentioned here is the second generated path data)

iv) *execution logic for conditionally executing the prefetch instruction based upon*

a comparison operation that compares the first path data to the second path data

to determine if the first path data falls within the predicted second path (column 6,

lines 33-36; canceling the prefetched request is the same as conditionally

executing a prefetch instruction)

In regard to claim 13, Yeh taught the limitation *wherein the first path data is*

derived from a compiler performing static compilation (column 4, lines 49-53; column 6,

lines 21-27).

In regard to claim 14, Yeh taught the limitation *wherein the second path data is*

derived from information characterizing dynamic execution of the sequence of

instructions by the one processor unit (column 6, lines 28-33; second path is the

execution path).

In regard to claim 15, Yeh taught *wherein the execution logic executes the*

prefetch instruction upon determining that the first path falls within the predicted second

path (column 6, lines 28-37; the unneeded prefetch requests are cancelled and in this

manner only the prefetch instruction which is actually needed is then executed).

In regard to claim 16, Yeh taught *wherein the execution logic omits execution of the prefetch instruction upon determining that the first path does not fall within the predicted second path* (column 6, lines 28-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10.   Claims 6-9, 11, 17-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (USPN 5,742,804).

In regard to claim 6, Yeh taught the limitation *wherein the second path data are associated with one or more branch instructions* (column 6, lines 13-18; column 6, lines 28-33; Figure 1). Yeh does not explicitly state the limitation *wherein the second path data comprises a mask that represents a predicted path of execution that follows the associated branch instructions.* Though, in view of column 6, lines 7-20; column 6, lines 28-37, a masking pattern is being used for the first path, and one of ordinary skill in the art would recognize implementing Yeh's execution path (the second path) in the same bit pattern (i.e. "mask" indicating the path) would make the mentioned comparison operation easier. It would be a simple one-to-one comparison. Therefore, it would have been obvious to implement Yeh with a mask representing the path.

In regard to claim 7, Yeh taught the limitation *wherein the first path data comprises a mask that represents path of execution from the prefetch instruction to the instruction that uses the information prefetched by the prefetch instruction* (column 4, lines 43-57; column 6, lines 7-20; the bit encodings represent the mask, which represents the path).

In regard to claim 8, Yeh taught the limitation *wherein the second path data are based upon accumulation of predictions associated with branch instructions* (column 6, lines 13-18; column 6, lines 28-33).

In regard to claim 9, Yeh taught the limitation *wherein the second path data is derived from predictions based upon previous execution of the instruction stream* (column 6, lines 13-18; column 6, lines 28-33).

In regard to claims 11 and 22, Yeh taught the additional limitation *wherein the prefetch instruction includes a field that identifies data to prefetch from memory into the high speed buffer* (column 4, line 6; target field identifies the data to be prefetched). Yeh did not explicitly state the limitation *wherein the data is operated on by at least one instruction in the instruction stream*. However, Yeh did allude to this concept of the prefetch instruction prefetching data to be operated on in column 1, lines 22-25. Here, Yeh states both instructions and data are needed to keep the computer running efficiently. Clearly if the instructions are being prefetched, the data for those

instructions would need to be prefetched as well in order to keep up with the continual

stream of operation. It would not make sense to have instructions prepared for

execution in a cache and then have those same instructions wait for data. If the

compiler knows what instructions are going to be executed it can also make a guess as

to what data those instructions will need. Therefore, it would have been obvious to one

of ordinary skill in the art to implement Yeh with an ability to add a branch predict (data

prefetch) instruction in the instruction stream for the purpose of preparing data for use in

a predicted future path in order to provide smooth and efficient prefetched data and

instruction operations to the cache and thus to the processor.

In regard to claim 17, Yeh taught the additional limitation *wherein the second*

path data are associated with one or more branch instructions (column 6, lines 13-18;

column 6, lines 28-33; Figure 1). Yeh does not explicitly state *wherein the second path*

data comprises a mask that represents a predicted path of execution that follows the

associated branch instructions. Though, in view of column 6, lines 7-20; column 6, lines

28-37, a masking pattern is being used for the first path, and one of ordinary skill in the

art would recognize implementing Yeh's execution path (the second path) in the same

bit pattern (i.e. "mask" indicating the path) would make the mentioned comparison

operation easier. It would be a simple one-to-one comparison. Therefore, it would have

been obvious to implement Yeh with a mask representing the path.

In regard to claim 18, Yeh taught the limitation *wherein the first path data comprises a mask that represents path of execution from the prefetch instruction to the instruction that uses the information prefetched by the prefetch instruction* (column 4, lines 43-57; column 6, lines 7-20; the bit encodings represent the mask, which represents the path).

In regard to claim 19, Yeh taught the limitation *further comprising branch prediction logic for generating predictions associated with branch instructions, and a branch history queue for accumulating the predictions generated by the branch prediction logic, wherein the second path data generated by the path prediction logic is based upon the predictions accumulated in the branch history queue* (column 6, lines 13-18; column 6, lines 28-33). Of particular importance is the branch history queue, which is not explicitly stated in the above referenced passages, however it would have been obvious to one of ordinary skill that such a structure exists inherently in Yeh since some method of recording the branch histories is needed for prediction purposes.

In regard to claim 20, Yeh taught the limitation *wherein the predictions are based upon previous execution of the instruction stream* (column 6, lines 13-18; column 6, lines 28-33).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to

a rejection of claims, the patentable novelty must be clearly shown in view of the state

of the art disclosed by the references cited and the objections made. Applicant must

also show how the amendments avoid such references and objections. See 37 CFR §

1.111(c).

Dubey (USPN 5,774,685) taught a prefetch instruction composed of a mask and

manipulated at compile time for the purpose of moving up the branch tree structure.

The limitation Dubey did not present was conditionally executing the prefetch

instruction.

Sharangpani et al. (USPN 6,065,115) taught a method of conditionally executing

branch paths based upon past history of the branch instructions. This is of particular

relevance to the claims and limitations concerning conditionally executing the prefetch

instruction ahead of time./

McInerney et al. (USPN 6,212,603) taught a trace vector for storing information

pertaining to branch path history.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to William H. Wood whose telephone number is (703)305-

3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday
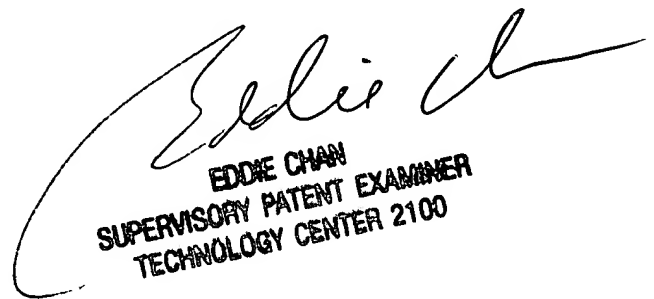
and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone numbers for

the organization where this application or proceeding is assigned are (703)746-7239 for

regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703)305-

3900.

William H. Wood
June 17, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100